

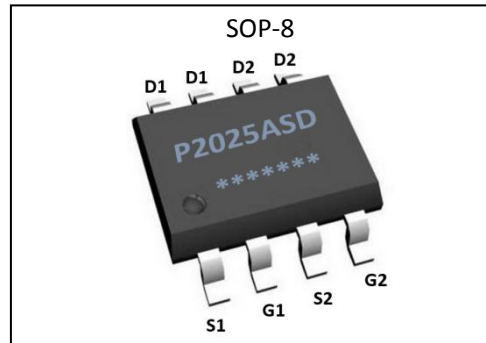
General Description :

The HMP2025ASD uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOP-8, which accords with the RoHS standard.

V_{DSS}	-20	V
I_D	-8	A
P_D	3.0	W
$R_{DS(ON)type}$	19	m Ω

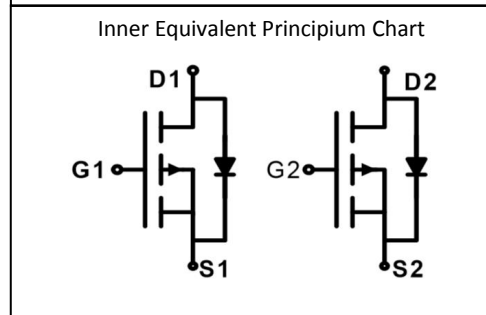
Features :

- $R_{DS(ON)} < 25m\Omega @ V_{GS}=4.5V$ (Typ 19m Ω)
- High density cell design for ultra-low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation



Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Package Marking and Ordering Information:

Device Marking	Device	Device Package	Quantity
P2025ASD	HMP2025ASD	SOP-8	4000 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	-20	V
I_D	Continuous Drain Current	-8	A
I_{DM}	Pulsed Drain Current	-32	A
V_{GS}	Gate-to-Source Voltage	± 12	V
P_D	Power Dissipation	3.0	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	155 , -55 to 175	$^\circ C$

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	-20	--	--	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=-20V, V_{GS}=0V, T_a=25^\circ\text{C}$	--	--	-1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+12V$	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-12V$	--	--	-0.1	μA

ON Characteristics ^{a3}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	$V_{GS}=-4.5V, I_D=-6.5A$	--	19	25	$m\Omega$
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	$V_{GS}=-2.5V, I_D=-5.0A$	--	25	35	$m\Omega$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	-0.4	-0.65	-1.0	V

Pulse width $t_p \leq 380\mu s, \delta \leq 2\%$

Dynamic Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-6.5A$	8	--	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V$	--	1200	--	pF
C_{oss}	Output Capacitance	$V_{DS}=-10V$	--	310	--	
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	--	240	--	

Resistive Switching Characteristics ^{a4}						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-10V$	--	25	--	ns
t_r	Rise Time	$I_D=-1A$	--	30	--	
$t_{d(OFF)}$	Turn-Off Delay Time	$V_{GS}=-4.5V$	--	60	--	
t_f	Fall Time	$R_G=6.0\Omega$	--	45	--	
Q_g	Total Gate Charge	$V_{DD}=-10V$	--	10	--	nC
Q_{gs}	Gate to Source Charge	$I_D=-6.5A$	--	1.8	--	
Q_{gd}	Gate to Drain ("Miller") Charge	$V_{GS}=-4.5V$	--	3	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current ^{a2} (Body Diode)		--	--	-8	A
V_{SD}	Diode Forward Voltage ^{a3}	$I_S=-8A, V_{GS}=0V$	--	--	-1.2	V

Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient ^{a2}	40	°C/W

^{a1} : Repetitive Rating: Pulse width limited by maximum junction temperature.

^{a2} : Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

^{a3} : Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

^{a4} : Guaranteed by design, not subject to production

Characteristics Curve :

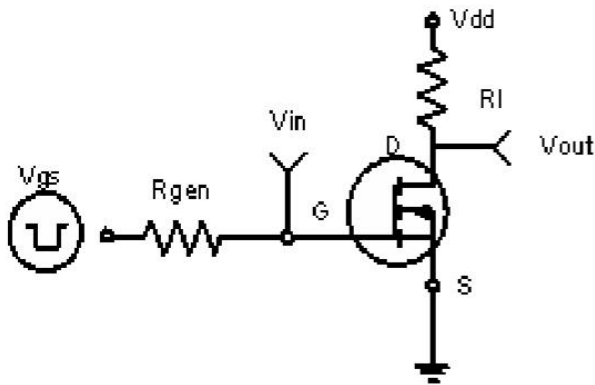


Figure 1 Switching Test Circuit

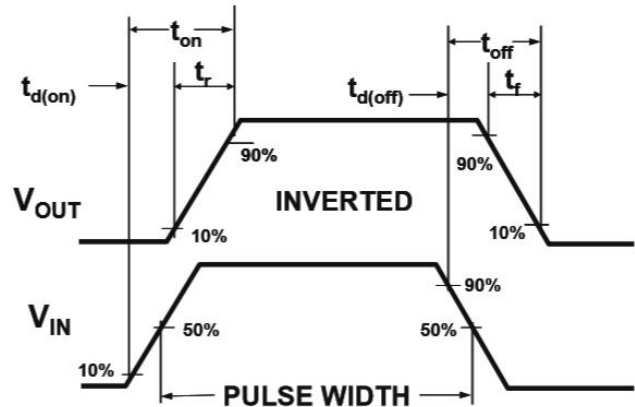


Figure 2 Switching Waveforms

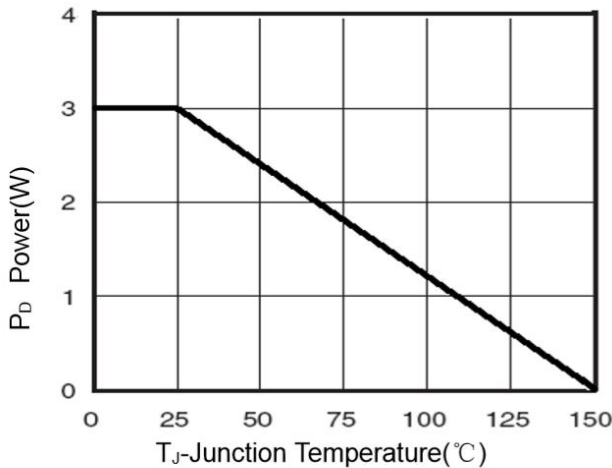


Figure 3 Power Dissipation

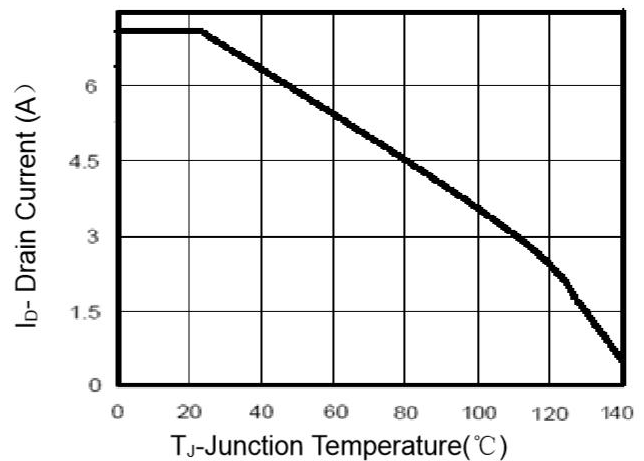


Figure 4 Drain Current

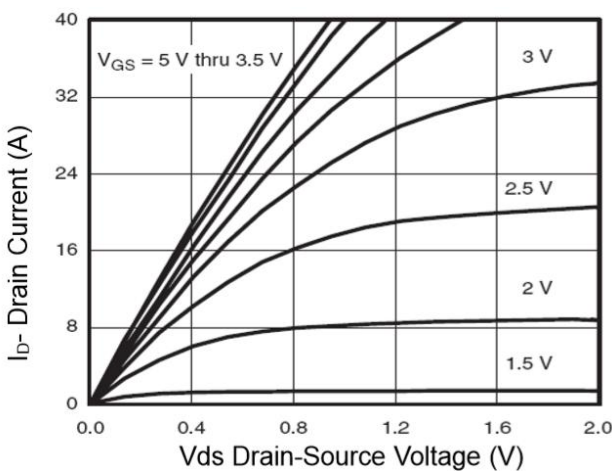


Figure 5 Output Characteristics

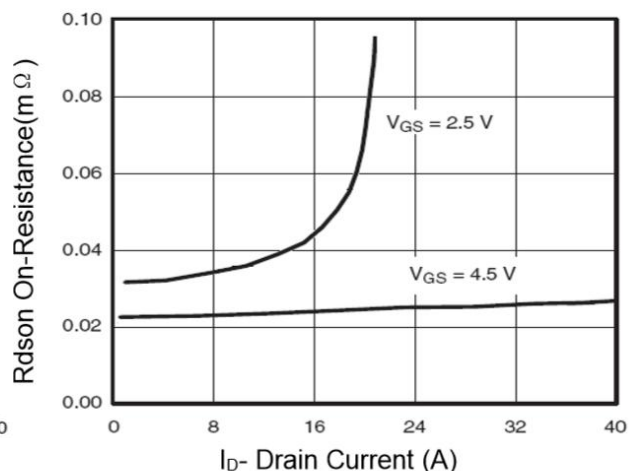


Figure 6 Drain-Source On-Resistance

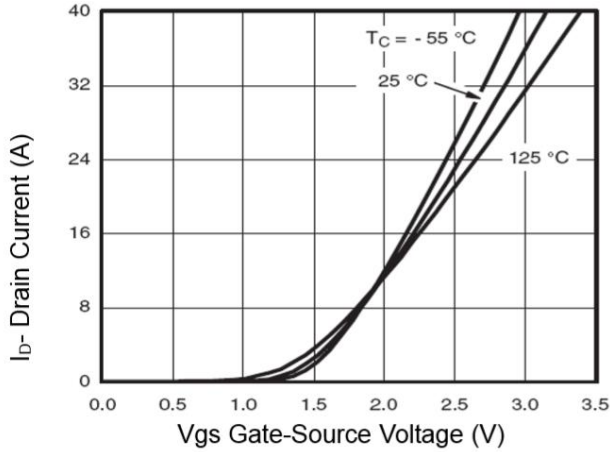


Figure 7 Transfer Characteristics

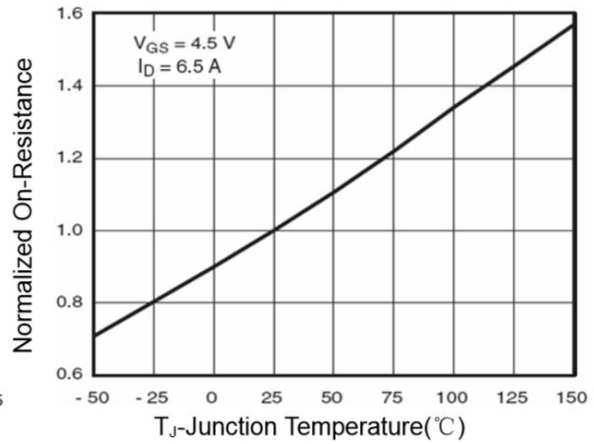


Figure 8 Drain-Source On-Resistance

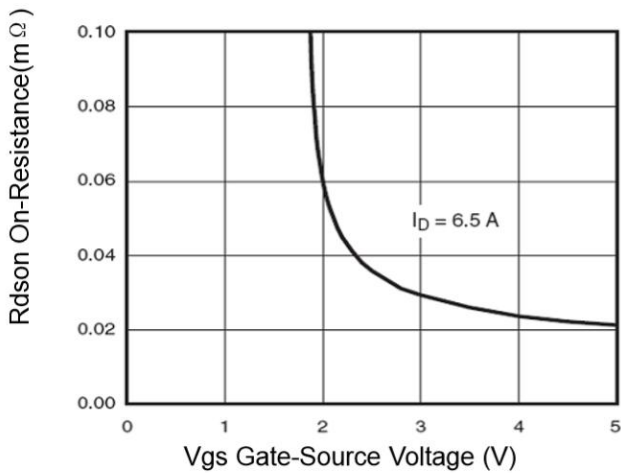


Figure 9 Rdson vs Vgs

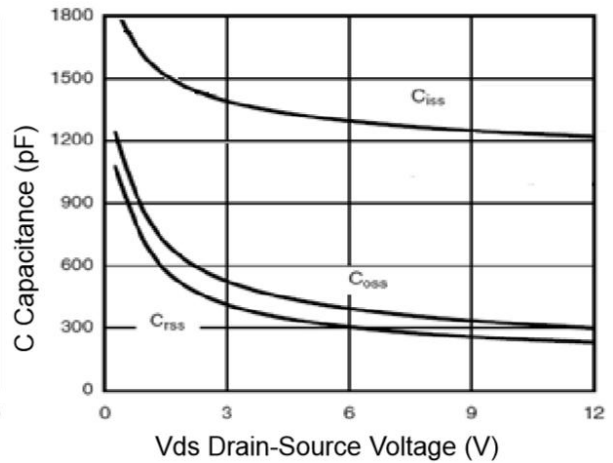


Figure 10 Capacitance vs Vds

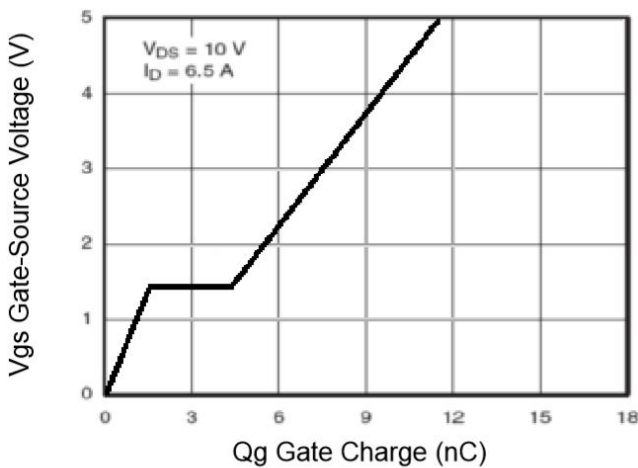


Figure 11 Gate Charge

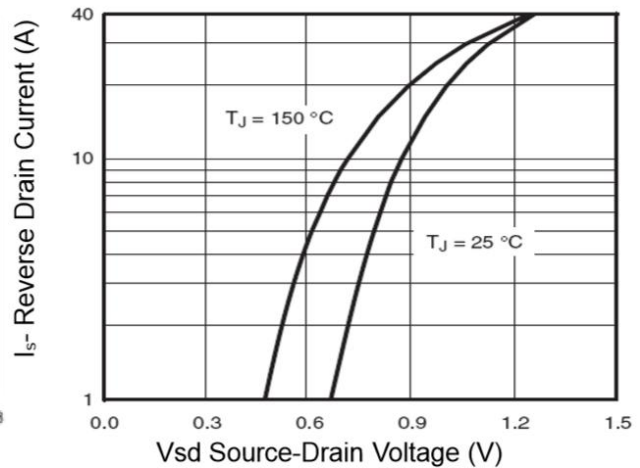


Figure 12 Source- Drain Diode Forward

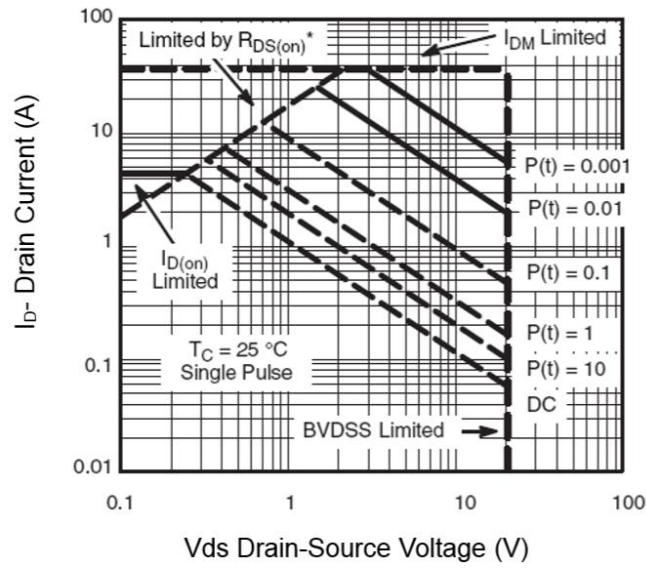


Figure 13 Safe Operation Area

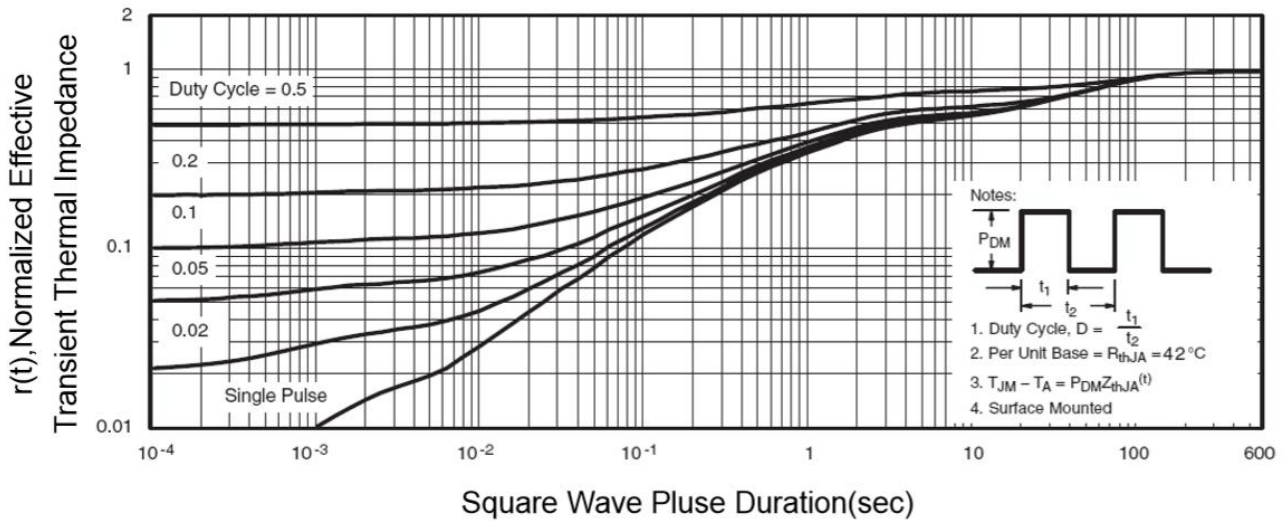
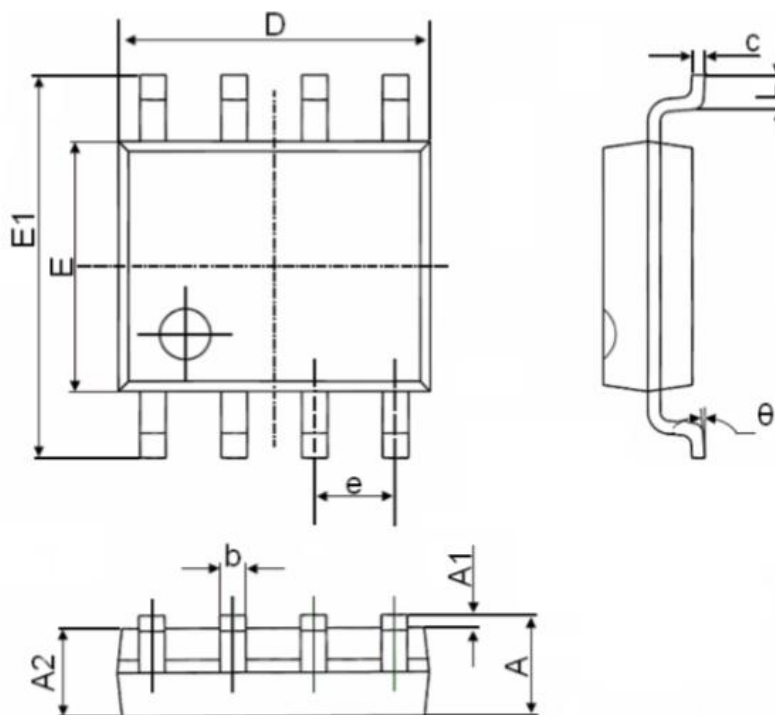


Figure 14 Normalized Maximum Transient Thermal Impedance

Marking Information

	Part	NO.
●	Y M	W SN
Part NO.	HMP2025ASD	
●	Pin 1 Indicator	
Lot NO.	Y : Year ; M : Month ; W : Week ; SN : Pipeline Code	

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



HMP2025ASD

HM Silicon P-Channel Power MOSFET

Revision History

Revision	Date	Descriptions
REV.1.0	Sep, 2019	Initial Version